UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
WASHINGTON, D.C. 20549

FORM 6-K

REPORT OF FOREIGN PRIVATE ISSUER
PURSUANT TO RULE 13a-16 OR 15d-16 UNDER
THE SECURITIES EXCHANGE ACT OF 1934

For the month of December 2024

Commission File Number: 001-41426

Nano Labs Ltd
(Exact name of registrant as specified in its charter)

China Yuangu Hanggang Technology Building
509 Qianjiang Road, Shangcheng District,
Hangzhou, Zhejiang, 310000
People's Republic of China
(Address of principal executive offices)

Indicate by check mark whether the registrant files or will file annual reports under cover of Form 20-F or Form 40-F.

Form 20-F ☒ Form 40-F ☐

EXPLANATORY NOTE

The document attached as exhibit 99.1 to this Form 6-K is hereby incorporated by reference into the Registrant's Registration Statement on Form F-3 initially filed with the U.S. Securities and Exchange Commission on August 14, 2023 (Registration No. 333-273968) and shall be a part thereof from the date on which this current report is furnished, to the extent not superseded by documents or reports subsequently filed or furnished.

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

Nano Labs Ltd

Date: December 26, 2024

By: /s/ Jianping Kong
Name: Jianping Kong
Title: Chairman and Chief Executive Officer

EXHIBIT INDEX

Exhibit No.	Description
Exhibit 99.1	Press Release

Exhibit 99.1

Nano Labs Launches FPU3.0 ASIC Design Architecture with 3D DRAM Stacking for AI and Blockchain Innovation

Hong Kong, December 26, 2024 /PRNewswire/ — Nano Labs Ltd (Nasdaq: NA) ("we," the "Company," or "Nano Labs"), a leading fabless integrated circuit design company and product solution provider in China, today announced the launch of FPU3.0, an ASIC architecture designed to enhance artificial intelligence (AI) inference and blockchain performance. Featuring advanced 3D DRAM stacking technology, FPU3.0 delivers a fivefold boost in power efficiency over the previous FPU2.0 architecture, setting a new standard for energy-efficient, high-performance ASICs. This latest advancement highlights the Company's robust research and development capabilities in adopting cutting-edge technologies and its commitment to driving innovation and widespread adoption in the AI and cryptocurrency industry.

The FPU series represents Nano Labs' proprietary set of ASIC chip design architectures, purpose-built for high-bandwidth High Throughput Computing (HTC) applications. Such ASIC chips are optimized for specific functions or applications, typically delivering lower power consumption and higher computational efficiency than general-purpose CPUs and GP-GPUs. These ASICs are increasingly utilized in AI inference, edge AI computing, data transmission processing under 5G networks, network acceleration, and more.

The Nano FPU architecture comprises four fundamental modules and IPs: the Smart NOC (Network-on-Chip), the high-bandwidth memory controller, the chip-to-chip interconnect IOs, and the FPU core. This modular provides remarkable flexibility, enabling rapid product iteration by updating the FPU core IP while reusing or upgrading other IPs and modules as needed - often sufficient to introduce new features.

Notably, the FPU3.0 architecture incorporates stacked 3D memory with a theoretical bandwidth of 24TB/s and an upgraded Smart-NOC on-chip network. This network supports a mix of large and small compute cores, full-crossbar, and feed-through traffic types on the bus. The FPU3.0 architecture holds the potentials to excel in various fields, delivering superior performance, lower power consumption, and faster product iteration cycles.

About Nano Labs Ltd

Nano Labs Ltd is a leading fabless integrated circuit ("IC") design company and product solution provider in China. Nano Labs is committed to the development of high throughput computing ("HTC") chips, high performance computing ("HPC") chips, distributed computing and storage solutions, smart network interface cards ("NICs") vision computing chips and distributed rendering. Nano Labs has built a comprehensive flow processing unit ("FPU") architecture which offers solution that integrates the features of both HTC and HPC. Nano Lab's Cuckoo series are one of the first near-memory HTC chips available in the market*. For more information, please visit the Company's website at: ir.nano.cn.

* According to an industry report prepared by Frost & Sullivan.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, as amended, and *as defined in the U.S. Private Securities Litigation Reform Act of 1995. These forward-looking statements include, without limitation, the Company's plan to appeal the Staff's determination, which can be identified by terminology such as "may," "will," "expect," "anticipate," "aim," "estimate," "intend," "plan," "believe," "potential," "continue," "is/are likely to" or other similar expressions. Such statements are based upon management's current expectations and current market and operating conditions, and relate to events that involve known or unknown risks, uncertainties and other factors, all of which are difficult to predict and many of which are beyond the Company's control, which may cause the Company's actual results, performance or achievements to differ materially from those in the forward-looking statements. Further information regarding these and other risks, uncertainties or factors is included in the Company's filings with the Securities and Exchange Commission. The Company does not undertake any obligation to update any forward-looking statement as a result of new information, future events or otherwise, except as required under law.*

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